HYCON TECHNOLOGY

HY2540AA-T016-AC
Datasheet

Protection IC for 3/4-cell Li+ Battery

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1. General Description

HY2540AA-T016-AC is a protection IC for safety of 3-cell / 4-cell lithium ion and lithium polymer rechargeable batteries. The protection IC integrates accurate voltage detection and protection delay circuitry for best battery protection purpose.

2. Features

(1) High-accuracy voltage detection for each cell:

- Overcharge detection voltage n (n = 1 to 4) 4.350V Accuracy: ±25mV
- Overcharge release voltage n (n = 1 to 4) 4.150V Accuracy: ±50mV
- Overdischarge detection voltage n (n = 1 to 4) 2.400V Accuracy: ±80mV
- Overdischarge release voltage n (n = 1 to 4) 3.000V Accuracy: ±100mV

(2) Charge overcurrent protection:

- Charge overcurrent detection voltage -0.100V Accuracy: ±25mV

(3) Three-level discharge overcurrent protection:

- Overcurrent detection voltage 1 0.200V Accuracy: ±25mV
- Overcurrent detection voltage 2 0.500V Accuracy: ±50mV
- Overcurrent detection voltage 3 VC1-1.2V Accuracy: ±300mV

(4) Delay time:

Delay times are set by external capacitors respectively at CCT pin and CDT pin for overcharge detection, /charge overcurrent detection and overdischarge detection/discharge overcurrent detection voltage 1. Delay times are set internally for discharge overcurrent detection voltage 2 (1ms) and discharge overcurrent detection 3 (300μs).

(5) Cell number selection:

SEL pin is used to select either 3 battery cells in use or 4 battery cells in use.

(6) Charge/discharge operation can be controlled via the CTL pin.

(7) 0V Battery Charge function：available.

(8) High voltage withstand range: Absolute maximum rated level: 28V

(9) Wide operating voltage range: Maximum operation voltage level: 26V

(10) Wide operating temperature range: -40℃ to +85℃

(11) Low current consumption

- Operation mode 12μA typ., 30μA max. (V_{Cn} = 3.5V)
- Power-down mode 1.2μA typ., 2.0μA max. (V_{Cn} = 2.0V)

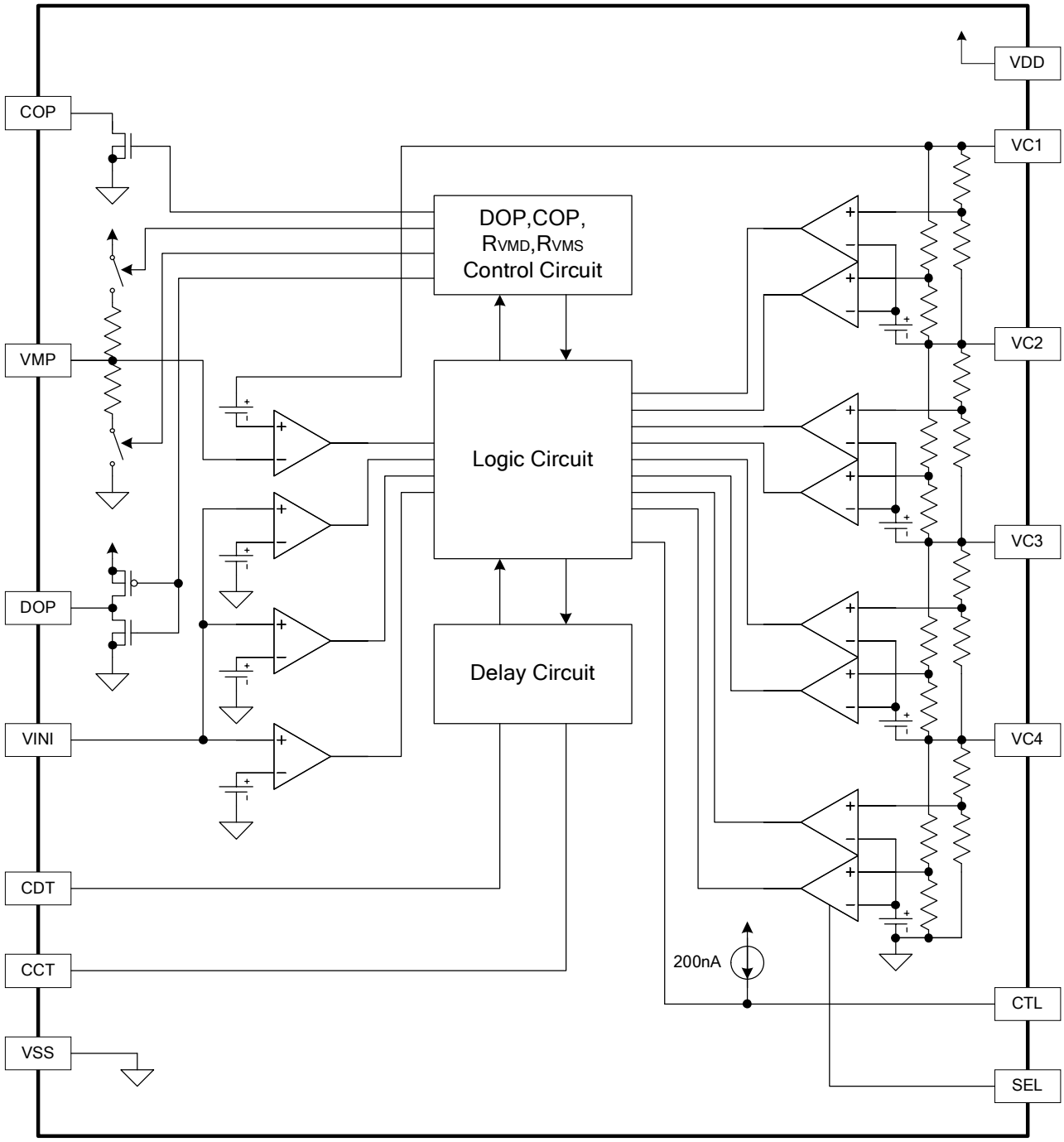
(12) Small package: 16-pin TSSOP

(13) Halogen free green product

3. Applications

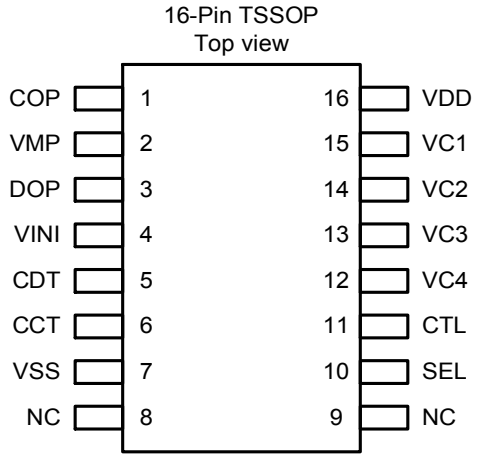
- 3-cell / 4-cell lithium ion rechargeable battery pack
- 3-cell / 4-cell lithium polymer rechargeable battery pack

4. Block Diagram



5. Pin definition

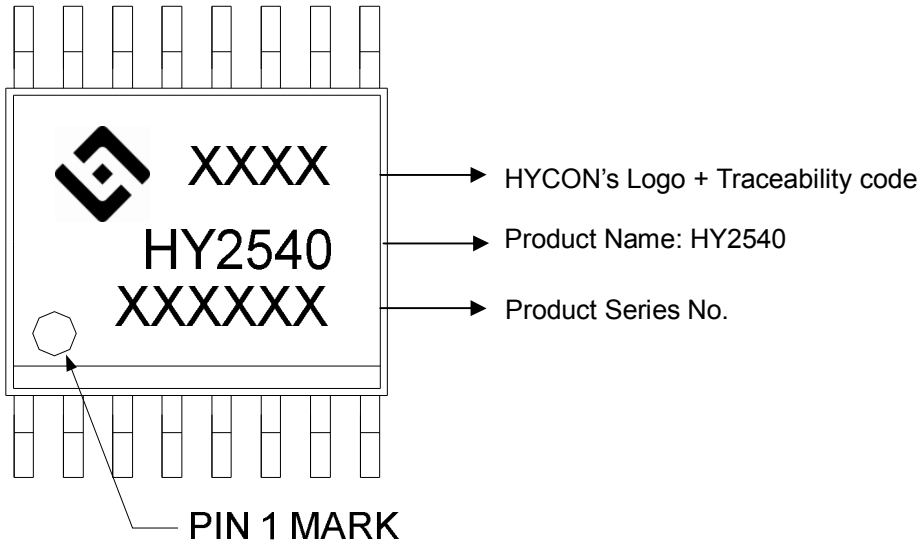
5.1. TSSOP-16 Diagram



5.2. pinout I/O Description

Pin	Symbol	Description
1	COP	FET gate connection pin for charge control (Nch open drain output)
2	VMP	Pin for voltage detection between VC1 and VMP (Pin for discharge overcurrent detection 3)
3	DOP	FET gate connection pin for discharge control FET (CMOS output)
4	VINI	Pin for voltage detection between VSS and VINI (Pin for discharge overcurrent detection 1,2 and charge overcurrent detection)
5	CDT	Capacitor connection pin for overdischarge delay and discharge overcurrent detection 1 delay.
6	CCT	Capacitor connection pin for overcharge delay and charge overcurrent detection delay.
7	VSS	Input pin for negative power supply, Connection pin for battery 4's negative voltage
8	NC	No connection
9	NC	No connection
10	SEL	Pin for switching 3-series or 4-series cell VSS level: 3-series cell, VDD level : 4-series cell
11	CTL	Control of charge FET and discharge FET
12	VC4	Connection pin for battery 3's negative voltage, Connection pin for battery 4's positive voltage
13	VC3	Connection pin for battery 2's negative voltage, Connection pin for battery 3's positive voltage
14	VC2	Connection pin for battery 1's negative voltage, Connection pin for battery 2's positive voltage
15	VC1	Connection pin for battery 1's positive voltage
16	VDD	Input pin for positive power supply, Connection pin for battery 1's positive voltage

5.3. Package marking information



6. Electrical Characteristics

6.1. Absolute Maximum Rating

(VSS = 0V, Ta=25℃ unless indicated otherwise)

Item	Symbol	Specification	Unit
Input voltage between VDD and VSS	V_{DS}	VSS-0.3 to VSS+28	V
VC1 pin input voltage	VC1	VC2-0.3 to VC2+5.5	V
VC2 pin input voltage	VC2	VC3-0.3 to VC3+5.5	V
VC3 pin input voltage	VC3	VC4-0.3 to VC4+5.5	V
VC4 pin input voltage	VC4	VSS-0.3 to VSS+5.5	V
VINI pin input voltage	VINI	VSS-0.3 to VSS+5.5	V
CTL pin input voltage	CTL	VSS-0.3 to VDD+0.3	V
SEL pin input voltage	SEL	VSS-0.3 to VDD+0.3	V
VMP Input pin voltage	VMP	VSS-0.3 to VSS+28	V
COP pin output voltage	COP	VSS-0.3 to VSS+28	V
DOP pin output voltage	DOP	VSS-0.3 to VDD+0.3	V
Operating Temperature Range	TOP	-40 to +85	℃
Storage Temperature Range	TST	-40 to +125	℃
Tolerant Power Consumption	PD	400	mW

6.2. Electrical Parameters

(VSS = 0V, Ta=25℃ unless indicated otherwise)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection Voltage						
Overcharge detection voltage n (n = 1 to 4)	V_{CUn}		4.325	4.350	4.375	V
Overcharge release voltage n (n = 1 to 4)	V_{CRn}		4.100	4.150	4.200	V
Overdischarge detection voltage n (n = 1 to 4)	V_{DLn}		2.320	2.400	2.480	V
Overdischarge release voltage n (n = 1 to 4)	V_{DRn}		2.900	3.000	3.100	V
Overcurrent detection voltage 1	V_{IOV1}		0.175	0.200	0.225	V
Overcurrent detection voltage 2	V_{IOV2}		0.450	0.500	0.550	V
Overcurrent detection voltage 3	V_{IOV3}		VC1-1.5V	VC1-1.2V	VC1-0.9V	V
Charge overcurrent detection voltage	V_{CIP}		-0.125	-0.100	-0.075	V
Temperature coefficient for overcharge detection voltage	TC_{OE1}	Ta = 0℃~ 50℃*1	-1	0	1	mV/℃
Temperature coefficient for overcurrent detection voltage 1	T_{COE2}	Ta = 0℃~ 50℃*1	-0.5	0	0.5	mV/℃
Delay Time						
Overcharge detection delay time	T_{OC}	CCT pin capacitance=0.1μF	0.5	1	1.5	s
Overdischarge detection delay time	T_{OD}	CDT pin capacitance=0.1μF	50	100	150	ms
Overcurrent detection delay time 1	T_{IOV1}	CDT pin capacitance=0.1μF	5	10	15	ms
Overcurrent detection delay time 2	T_{IOV2}		0.4	1	1.6	ms
Overcurrent detection delay time 3	T_{IOV3}	FET gate capacitance = 2000pF.	100	300	600	μs
Charge overcurrent detection delay time	T_{CIP}	CCT pin capacitance=0.1μF	5	10	15	ms
0V Battery Charge Function(AVAILABLE)						
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charging available	3.0	-	-	V
Internal Resistance						
Resistance between VMP and VDD	R_{VMD}		0.5	1	1.5	MΩ
Resistance between VMP and VSS	R_{VMS}		0.45	0.9	1.8	MΩ

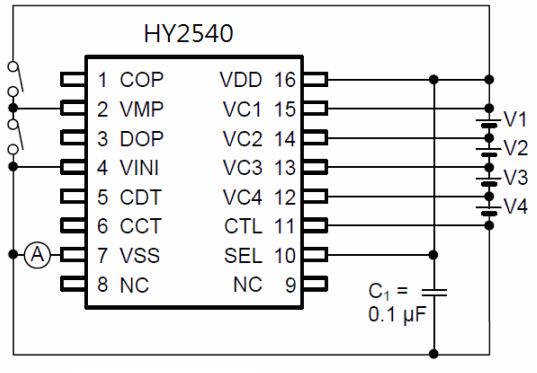
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Voltage						
Operating voltage between VDD and VSS	V_{DSOP}		3	-	26	V
CTL input voltage “H”	V_{CTLH}		4.0	-	-	V
CTL input voltage “L”	V_{CTLL}		-	-	2.0	V
SEL input voltage “H”	V_{SELH}		4.0	-	-	V
SEL input voltage “L”	V_{SELL}		-	-	2.0	V
Input Current						
Current consumption during operation	I_{OPE}	V1=V2=V3=V4=3.5V	-	12	30	μA
Current consumption during power-down	I_{PDN}	V1=V2=V3=V4=2.0V	-	1.0	2.0	μA
VC1 pin current	I_{VC1}	V1=V2=V3=V4=3.5V		3.6	6.0	μA
VC2 pin current	I_{VC2}	V1=V2=V3=V4=3.5V	-0.3	0	0.3	μA
VC3 pin current	I_{VC3}	V1=V2=V3=V4=3.5V	-0.3	0	0.3	μA
VC4 pin current	I_{VC4}	V1=V2=V3=V4=3.5V	-0.3	0	0.3	μA
CTL pin current “H”	I_{CTLH}	V1=V2=V3=V4=3.5V, CTL=VDD	-	-	0.1	μA
CTL pin current “L”	I_{CTLL}	V1=V2=V3=V4=3.5V, CTL=VSS	-0.6	-0.2	-	μA
SEL pin current “H”	I_{SELH}	V1=V2=V3=V4=3.5V, SEL=VDD	-	-	0.1	μA
SEL pin current “L”	I_{SELL}	V1=V2=V3=V4=3.5V, SEL=VSS	-0.1	-	-	μA
Output Current						
COP pin leakage current	I_{COH}	V_{COP}=26V	-	-	0.1	μA
COP pin sink current	I_{COL}	V_{COP}=VSS+0.5V	10	-	-	μA
DOP pin source current	I_{DOH}	V_{DOP}=VDD-0.5V	10	-	-	μA
DOP pin sink current	I_{DOL}	V_{DOP}=VSS+0.5V	10	-	-	μA

*1. The parameters within this temperature range are design guarantee values instead of screened values from high, low temperature measurement.

7. Test condition and circuit

7.1. Current Consumption during Operation (I_{OPE}), Current Consumption during Power-down (I_{PDN})

(Test circuit 1)



Test Circuit 1

7.1.1. Current Consumption during Operation (I_{OPE})

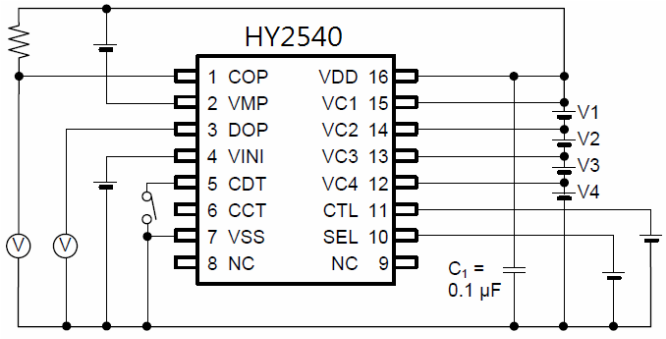
The current at the VSS pin when V1 = V2 = V3 = V4 = 3.5 V and V_{VMP} = VDD is the current consumption during operation (I_{OPE}).

7.1.2. Current Consumption during Power-down (I_{PDN})

The current at the VSS pin when V1 = V2 = V3 = V4 = 2.0 V, and VVMP=VSS is the current consumption during power-down (I_{PDN}).

7.2. Overcharge Detection Voltage (V_{CUn}), Overcharge Release Voltage (V_{CRn}), Overdischarge Detection Voltage (V_{DLn}), Overdischarge Release Voltage (V_{DRn}), Overcurrent Detection Voltage 1 (V_{IOV1}), Overcurrent Detection Voltage2 (V_{IOV2}), Overcurrent Detection Voltage3 (V_{IOV3}), CTL Input Voltage "H", CTL Input Voltage "L", SEL Input Voltage "H", SEL Input Voltage "L"

(Test Circuit 2)



Test Circuit 2

7.2.1. Overcharge Detection Voltage (V_{CUn}), Overcharge Release Voltage (V_{CRn})

The overcharge detection voltage (V_{CUn}) is the voltage of V1 when the voltage of the COP pin is “H” (VDD x 0.9 V or more) after the V1 voltage has been gradually increased starting at the initial status. The overcharge release voltage (V_{CRn}) is the voltage of V1 when the voltage at the COP pin is “L” after the V1 voltage has been gradually decreased.

7.2.2. Overdischarge Detection Voltage (V_{DLn}), Overdischarge Release Voltage (V_{DRn})

The overdischarge detection voltage (V_{DLn}) is the voltage of V1 when the voltage of the DOP pin is after the V1 voltage has been gradually decreased starting at the initial status. The overdischarge release voltage (V_{DRn}) is the voltage of V1 when the voltage at the DOP pin is “L” after the V1 voltage has been gradually increased.

When the voltage of Vn (n = 2 to 4) is changed, the overcharge detection voltage (V_{CUn}), overcharge release voltage (V_{CRn}), overdischarge detection voltage (V_{DLn}), and overdischarge release voltage (V_{DRn}) can be determined in the same way as when n = 1.

7.2.3. Overcurrent Detection Voltage1 (V_{IOV1})

Overcurrent detection voltage 1 (V_{IOV1}) is the voltage of the VINI pin when the voltage of the DOP pin1 (V_{IOV1}) is “H” after the VINI pin voltage has been gradually increased starting at the initial status.

7.2.4. Overcurrent Detection Voltage2 (V_{IOV2})

Overcurrent detection voltage 2 (V_{IOV2}) is the voltage of the VINI pin when the voltage of the DOP pinis “H” after the voltage of the CDT pin was set to V_{SS} following the initial status and the voltage of the VINI pin has been gradually decreased.

7.2.5. Overcurrent Detection Voltage3 (V_{IOV3})

Overcurrent detection voltage 3 (V_{IOV3}) is the voltage difference between V_{VC1} and V_{VMP} (V_{VC1} - V_{VMP}) when the voltage of the DOP pin is “H” after the VMP voltage has been gradually decreased starting at the initial status.

7.2.6. Overcharge Current Detection Voltage (V_{CIP})

Overcharge current detection voltage 1 (V_{CIP}) is the voltage of the VINI pin when the voltage of the COP pin1 (V_{CIP}) is “H” after the VINI pin voltage has been gradually increased starting at the initial status.

7.2.7. CTL Input Voltage “H” (V_{CTLH}), CTL Input Voltage “L” (V_{CTLL})

The CTL input voltage “H” (V_{CTLH}) is the voltage of CTL when the voltages at the COP and DOP pins are “H” after the CTL voltage has been gradually increased starting at the initial status. The CTL input voltage “L” (V_{CTLL}) is the voltage of CTL when the voltages at the COP

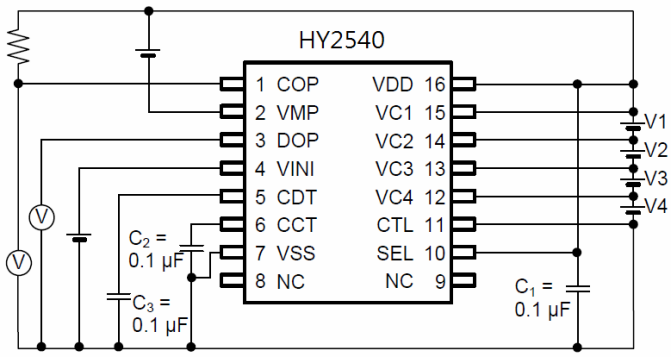
and DOP pins are “L” after the CTL voltage has been gradually decreased.

7.2.8. SEL Input Voltage “H” (V_{SELH}), SEL Input Voltage “L” (V_{SELL})

Apply 0 V to V4 in the initial status and confirm that the DOP pin is “H”. The SEL input voltage “L” (V_{SELL}) is the voltage of the SEL pin when the voltage at the DOP pin is “L” after the SEL voltage has been gradually decreased. The SEL input voltage “H” (V_{SELH}) is the voltage of the SEL pin when the voltage of the DOP pin is “H” after the SEL voltage has been gradually increased.

7.3. Overcharge Detection Delay Time (T_{OC}), Overdischarge Detection Delay Time (T_{OD}), Overcurrent Detection Delay Time 1 (T_{IOV1}), Overcurrent Detection Delay Time 2 (T_{IOV2}), Overcurrent Detection Delay Time 3 (T_{IOV3})

(Test Circuit 3)



Test Circuit 3

7.3.1. Overcharge Detection Delay Time (T_{OC})

The overcharge detection delay time (T_{OC}) is the time it takes for the voltage of the COP pin to change from “L” to “H” after the voltage of V1 is instantaneously changed to 4.5 V from the initial status.

7.3.2. Overdischarge Detection Delay Time (T_{OD})

The overdischarge detection delay time (T_{OD}) is the time it takes for the voltage of the DOP pin to change from “L” to “H” after the voltage of V1 is instantaneously changed to 1.5 V from the initial status.

7.3.3. Overcurrent Detection Delay Time1 (T_{IOV1})

Overcurrent detection delay time 1 (T_{IOV1}) is the time it takes for the voltage of the DOP pin to change from “L” to “H” after the voltage of the VINI pin is instantaneously changed to 0.4 V from the initial status.

7.3.4. Overcurrent Detection Delay Time2 (T_{IOV2})

Overcurrent detection delay time 2 (T_{IOV2}) is the time it takes for the voltage of the DOP pin to change from “L” to “H” after the voltage of the VINI pin is instantaneously changed to V_{IOV2} max. + 0.2 V from the initial status.

7.3.5. Overcurrent Detection Delay Time3 (T_{IOV3})

Overcurrent detection delay time 3 (T_{IOV3}) is the time it takes for the voltage of the DOP pin to change from “L” to “H” after the voltage of the VMP pin is instantaneously changed to V_{IOV3} min. - 0.2 V from the initial status.

8. Description of Operation

8.1. Normal Status

When the voltage of each of the batteries is in the range from V_{DLn} to V_{CUn} and the discharge current is lower than the specified value (the VINI pin voltage is higher than V_{CIP}, the VINI pin voltage is lower than V_{IOV1} and V_{IOV2}, and the VMP pin voltage is higher than V_{IOV3}), the charging and discharging FETs are turned on.

8.2. Overcharge Status

When the voltage of one of the batteries becomes higher than V_{CUn} and the state continues for T_{OC} or longer, the COP pin becomes high impedance. The COP pin is pulled up to the EB+ pin voltage by an external resistor, and the charging FET is turned off to stop charging. This is called the overcharge status. The overcharge status is released when one of the following two conditions holds.

(1) The voltage of each of the batteries becomes V_{CRn} or lower.

(2) The voltage of each of the batteries is V_{CUn} or lower, and the VMP pin voltage is 39 / 40 × VDD or lower (a load is connected and discharging is started via the body diode of the charging FET).

8.3. Overdischarge Status

When the voltage of one of the batteries becomes lower than V_{DLn} and the state continues for T_{OD} or longer, the DOP pin voltage becomes VDD level, and the discharging FET is turned off to stop discharging. This is called the overdischarge status.

8.4. Power-down Function

When the overdischarge status is reached, the VMP pin is pulled down to the VSS level by the internal R_{VMS} resistor of the IC. When the VMP pin voltage is 2.5V or lower, the power-down function starts to operate and almost every circuit in the HY2540AA-T016-AC stops working. The conditions of each output pin are as follows.

(1) COP pin : High-Z

(2) DOP pin : VDD

The power-down function is released when the following condition holds.

(1) The VMP pin voltage is 2.5V or higher.

The overdischarge status is released when the following two conditions hold.

(1) In case the VMP pin voltage is 2.5V or higher and the VMP pin voltage is lower than VDD, the overdischarge status is released when the voltage of each of the batteries is V_{DRn} or higher.

(2) In case a charger is connected, the overdischarge hysteresis is released. And the overdischarge status is released when the voltage of each of the batteries is V_{DLn} or higher.

8.5. Discharge Overcurrent Status

The HY2540AA-T016-AC has three overcurrent detection levels (V_{IOV1}, V_{IOV2}, and V_{IOV3}) and three overcurrent detection delay times (T_{IOV1}, T_{IOV2}, and T_{IOV3}) corresponding to each overcurrent detection level. When the discharging current becomes higher than the specified value (the voltage between VINI and VSS is greater than V_{IOV1}) and the state continues for T_{IOV1} or longer, the HY2540AA-T016-AC enters the overcurrent status, in which the DOP pin voltage becomes VDD level to turn off the discharging FET to stop discharging, the COP pin becomes high impedance and is pulled up to the EB+ pin voltage to turn off the charging FET to stop charging, and the VMP pin is pulled up to the VDD voltage by the internal resistor (R_{VMD}). Operation of overcurrent detection level 2 (V_{IOV2}) and overcurrent detection delay time 2 (T_{IOV2}) is the same as for V_{IOV1} and T_{IOV1}.

In the overcurrent status, the VMP pin is pulled up to the VDD level by the internal resistor in the IC (R_{VMD} resistor). The overcurrent status is released when the following condition holds.

(1) The VMP pin voltage is V_{IOV3} or higher because a charger is connected or the load (300 KΩ or more) is released.

8.6. Charge Overcurrent Status

The HY2540AA-T016-AC has charge overcurrent detection levels (V_{CIP}) and charge overcurrent detection delay times (T_{CIP}). When the charging current becomes higher than the specified value (the voltage between VINI and VSS is lower than V_{CIP}) and the state continues for T_{CIP} or longer, the HY2540AA-T016-AC enters the charge overcurrent status, the COP pin becomes high impedance. The COP pin is pulled up to the EB+ pin voltage by an external resistor, and the charging FET is turned off to stop charging.

The charge overcurrent status is released when the following condition holds.

(1) The VMP pin voltage is 39 / 40 × VDD or lower (disconnected the charger and a load is connected, discharging is started via the body diode of the charging FET).

8.7. 0 V Battery Charge Function

Regarding the charging of a self-discharged battery (0 V battery), When the charger voltage is higher than V_{0CHA}, the 0 V battery can be charged.

Caution When the VDD pin voltage is lower than the minimum value of V_{DSOP}, the operation of the HY2540AA-T016-AC is not guaranteed.

8.8. Delay Time Setting

The overcharge detection delay time (T_{OC}) and charge overcurrent delay time (T_{CIP}) are determined by the external capacitor connected to the CCT pin. The overdischarge detection delay time (T_{OD}) and overcurrent detection delay time 1 (T_{IOV1}) are determined by the external capacitor connected to the CDT pin. Overcurrent detection delay times 2 and 3 (T_{IOV2}, T_{IOV3}) are fixed internally.

	min.	typ.	max.	
T_{OC} [s]=	(5.00,	10.0,	15.0)	C_{CCT} [μF]
T_{OD} [s]=	(0.50,	1.00,	1.50)	C_{CDT} [μF]
T_{IOV1} [s]=	(0.05,	0.10,	0.15)	C_{CDT} [μF]
T_{CIP} [s]=	(0.05,	0.10,	0.15)	C_{CCT} [μF]

8.9. CTL Pin

The HY2540AA-T016-AC has control pins. The CTL pin is used to control the COP and DOP pin output voltages. CTL pin takes precedence over the battery protection circuit.

Conditions Set by CTL Pin

CTL Pin	COP Pin	DOP Pin
High	High-Z	VDD
Open	High-Z	VDD
Low	Normal status *1	Normal status *1

*1. The status is controlled by the voltage detector.

Caution Please note unexpected behavior might occur when electrical potential difference between the CTL pin ('L' level) and VSS is generated through the external filter (R_{VSS} and C_{VSS}) as a result of input voltage fluctuations.

8.10. SEL Pin

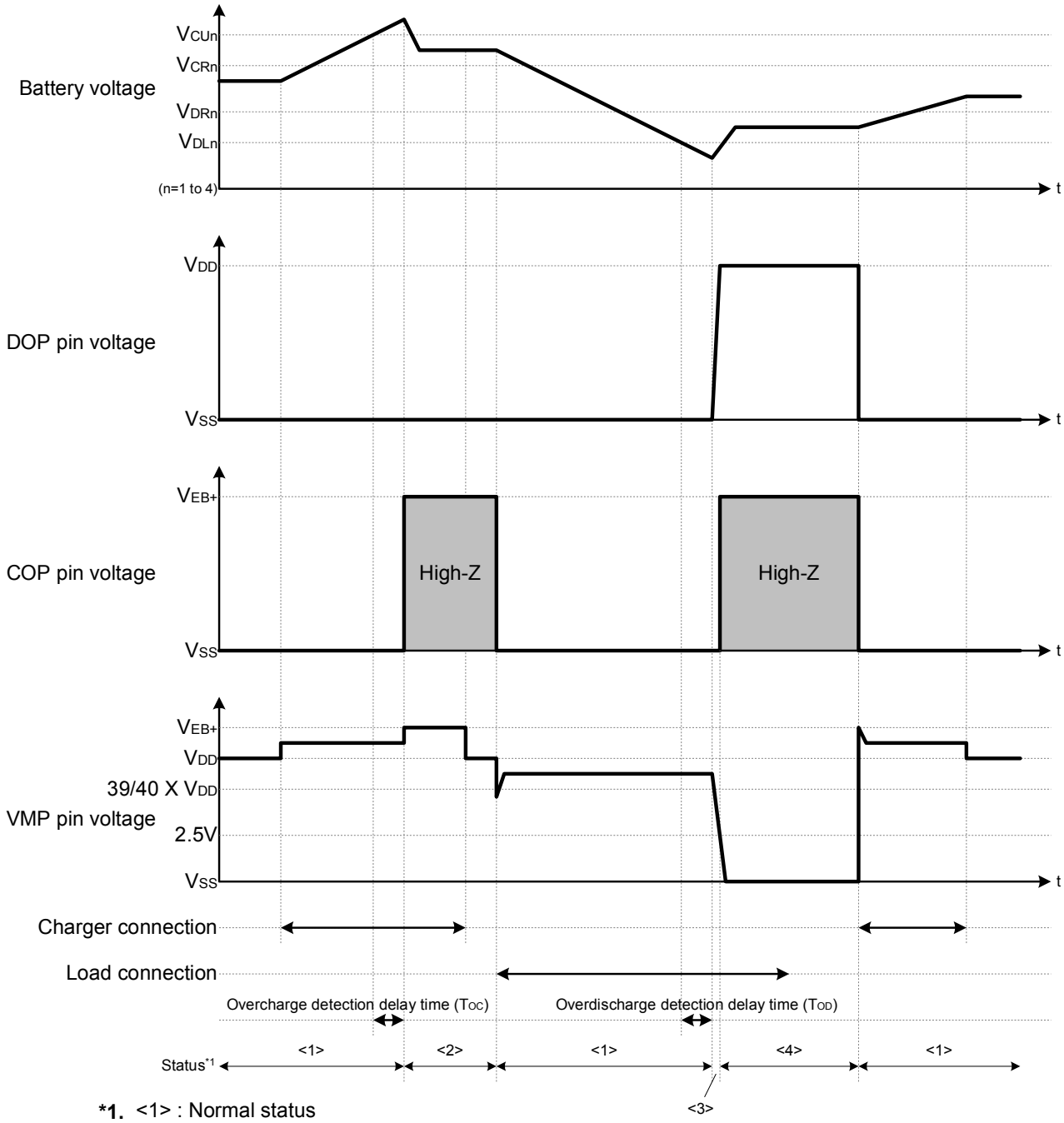
The HY2540AA-T016-AC Series has control pins. The SEL pin is used to switch between 3-cell and 4-cell protection. When the SEL pin is low, overdischarge detection of the V4 cell is prohibited and an overdischarge is not detected even if the V4 cell is shorted, therefore, the V4 cell can be used for 3-cell protection. The SEL pin takes precedence over the battery protection circuit. Use the SEL pin at high or low.

Conditions Set by SEL Pin

SEL Pin	Condition
High	4-cell protection
Open	Undefined
Low	3-cell protection

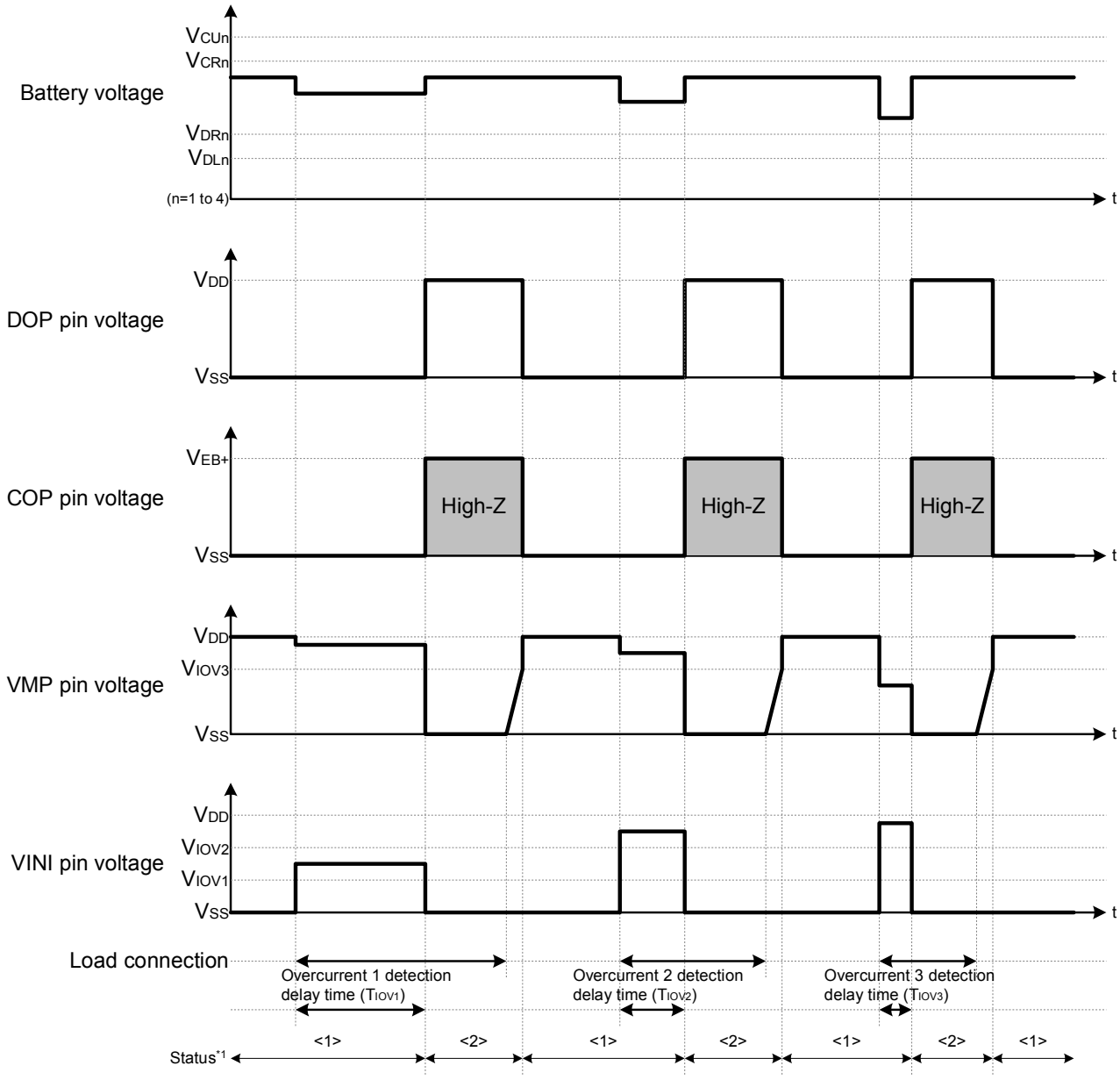
9. Timing Diagram

(1) Overcharge Detection and Overdischarge Detection



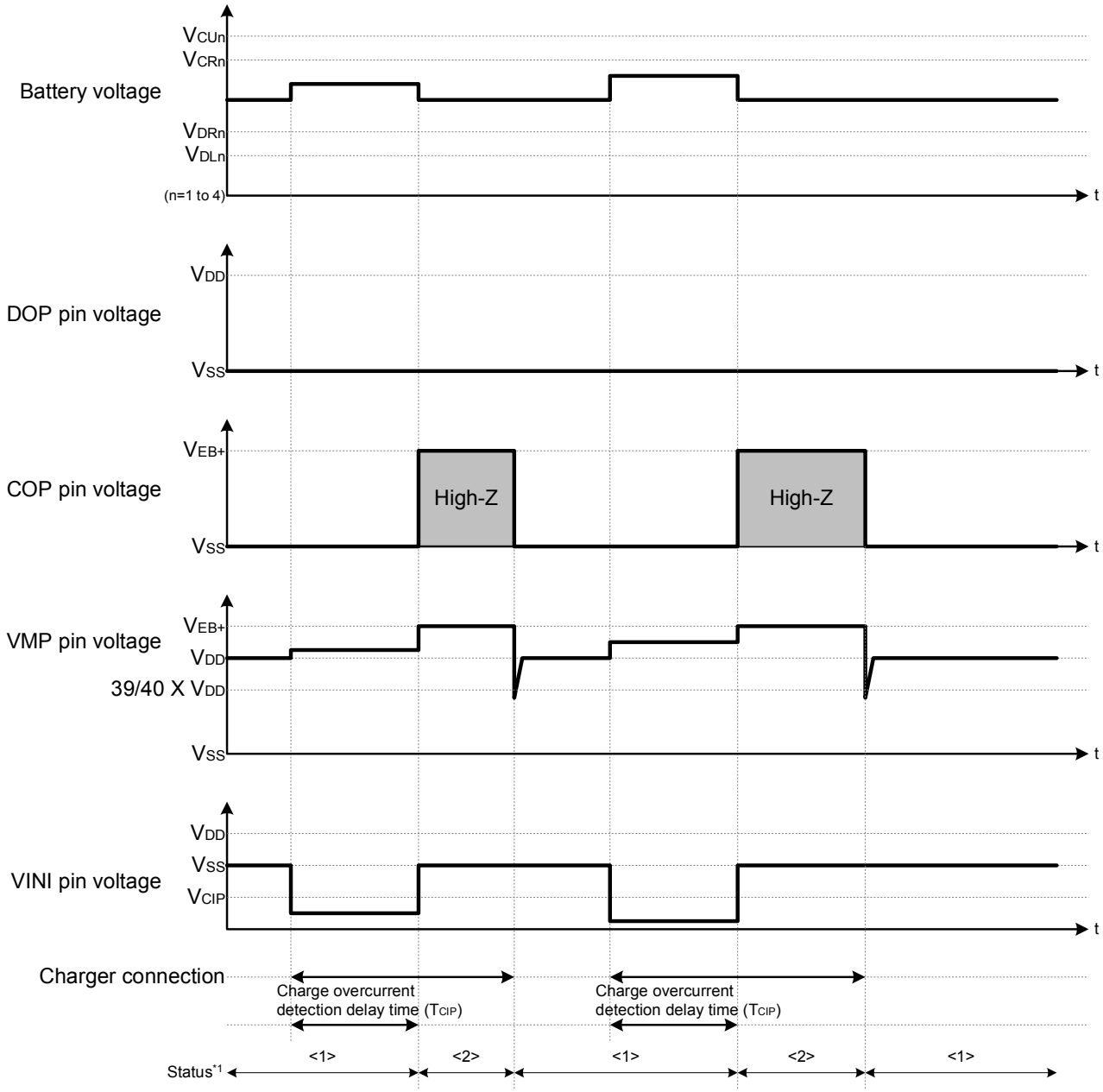
*1. <1> : Normal status
<2> : Overcharge status
<3> : Overdischarge status
<4> : Power-down status

(2) Discharge Overcurrent Detection



***1.** <1> : Normal status
<2> : Discharge overcurrent status

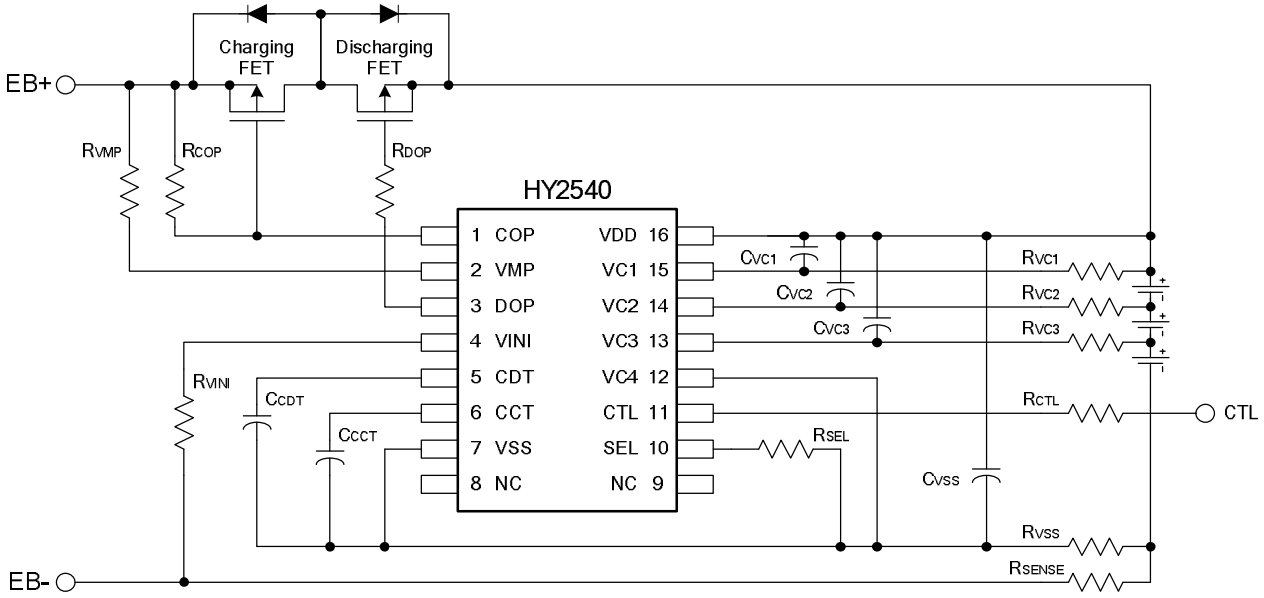
(3) Charge Overcurrent Detection



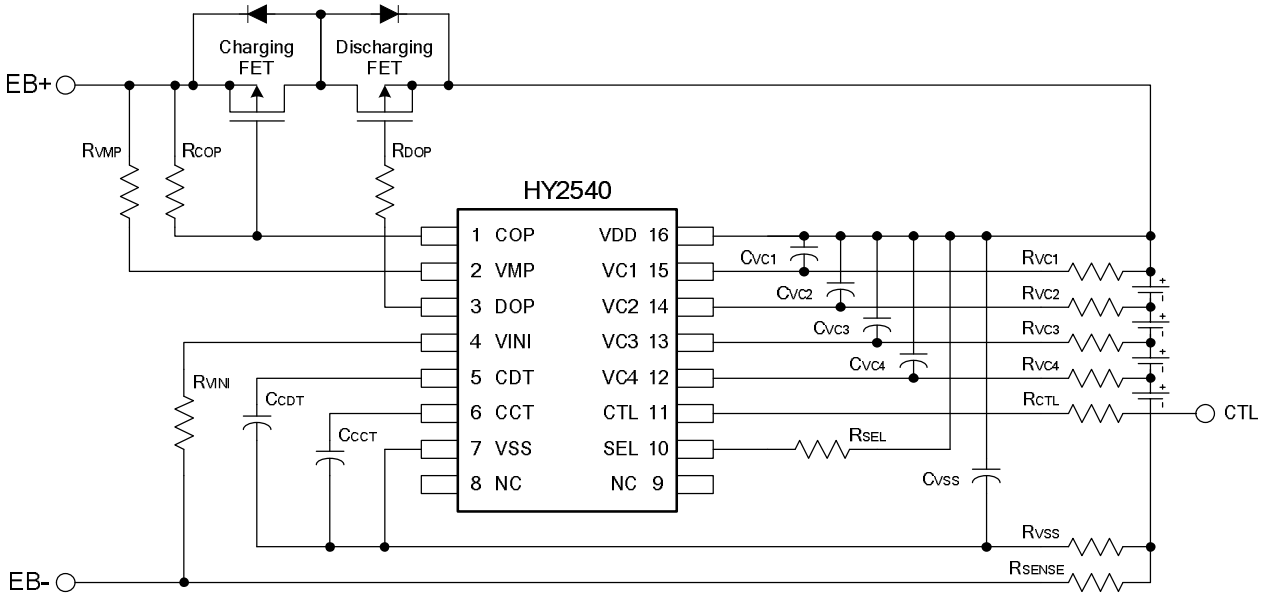
***1.** <1> : Normal status
<2> : Charge overcurrent status

10. Example of Application Circuit for Battery Protection IC

10.1. 3-serial Cell connection



10.2. 4-serial Cell connection



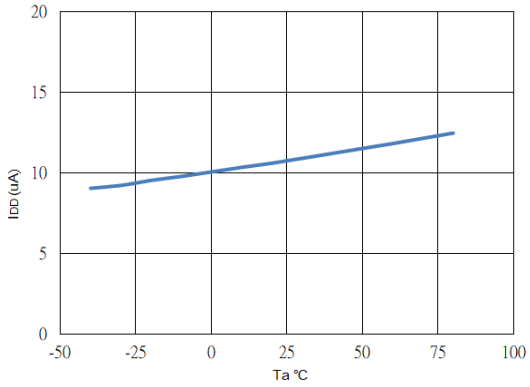
Symbol	Min.	Typ.	Max.	Unit	Remark
R_{VC1}	0	**1**	1	KΩ	*1
R_{VC2}	0	**1**	1	kΩ	*1
R_{VC3}	0	**1**	1	kΩ	*1
R_{VC4}	0	1	1	kΩ	*1
R_{DOP}	2	5.1	10	kΩ	
R_{COP}	0.1	1	1	kΩ	
R_{VMP}	1	5.1	10	kΩ	
R_{CTL}	1	1	100	kΩ	
R_{VINI}	1	1	100	kΩ	
R_{SEL}	1	1	100	kΩ	
R_{SENSE}	0	-	-	mΩ	
R_{VSS}	10	51	51	Ω	
C_{VC1}	0	0.1	0.33	μF	*1
C_{VC2}	0	0.1	0.33	μF	*1
C_{VC3}	0	0.1	0.33	μF	*1
C_{VC4}	0	0.1	0.33	μF	*1
C_{CCT}	0.01	0.1	-	μF	
C_{CDT}	0.07	0.1	-	μF	
C_{VSS}	2.2	2.2	10	μF	

Caution：

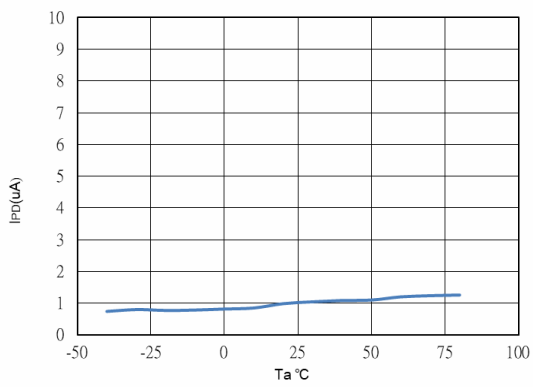
1. The above constants may be changed without notice, please download the most up-to-date datasheet on our website. http://www.hycontek.com
2. It is advised to perform thorough evaluation and test if peripheral devices need to be adjusted.

11. Temperature Characteristics (Typical Value)

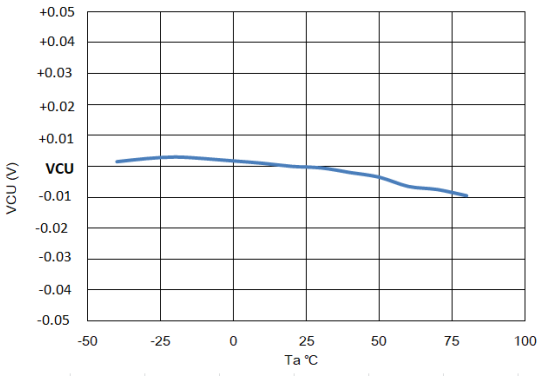
(1) I_{DD} vs. Ta



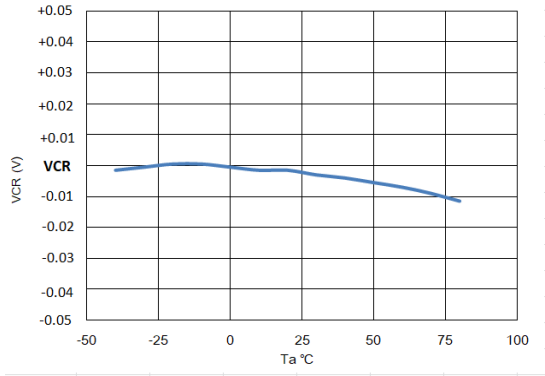
(2) I_{PD} vs. Ta



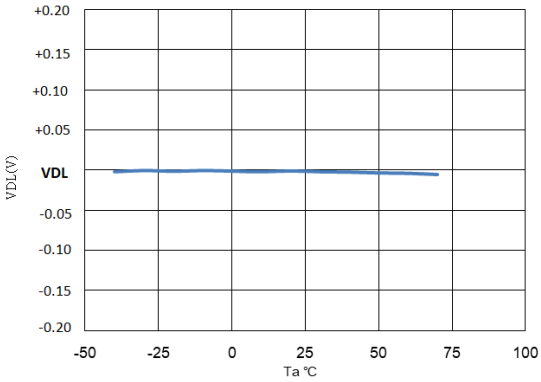
(3) V_{CUn} vs. Ta



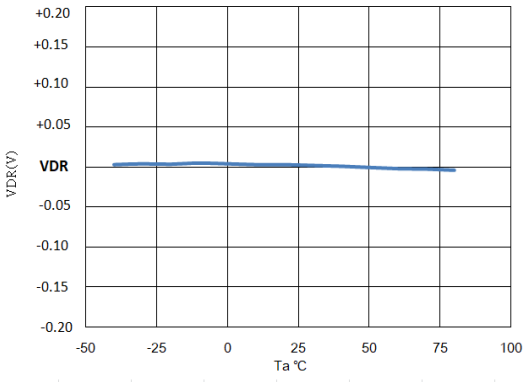
(4) V_{CRn} vs. Ta



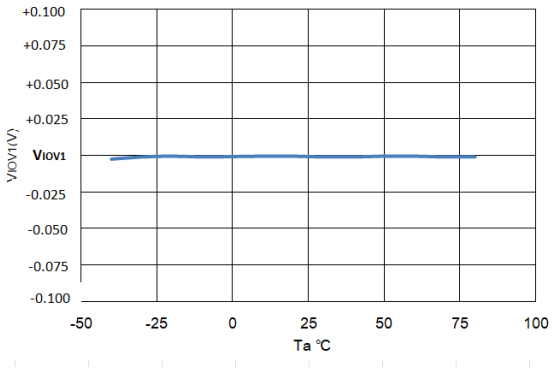
(5) V_{DLn} vs. Ta



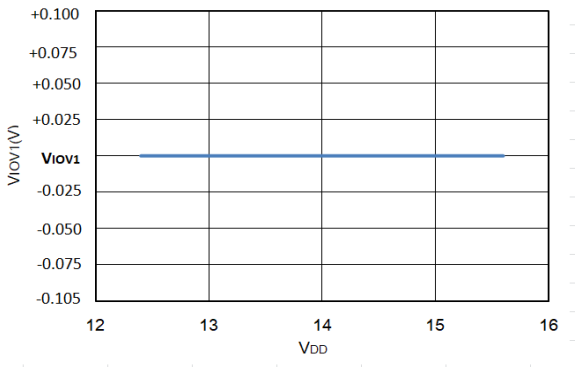
(6) V_{DRn} vs. Ta



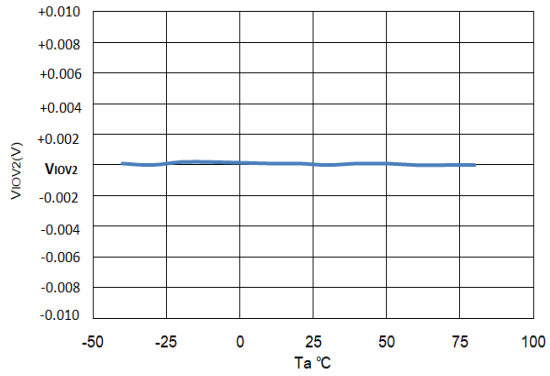
(7) V_{iov1} vs. Ta



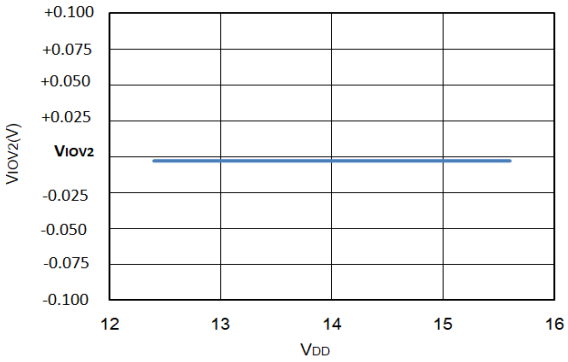
(8) V_{iov1} vs. VDD



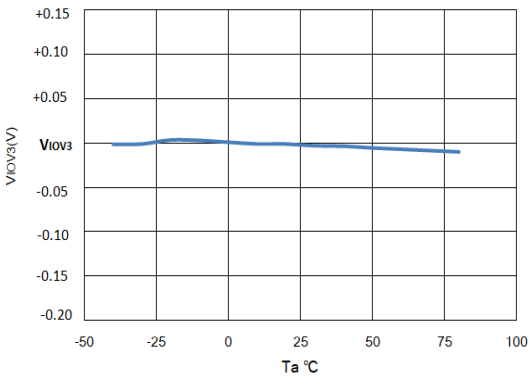
(9) V_{iov2} vs. Ta



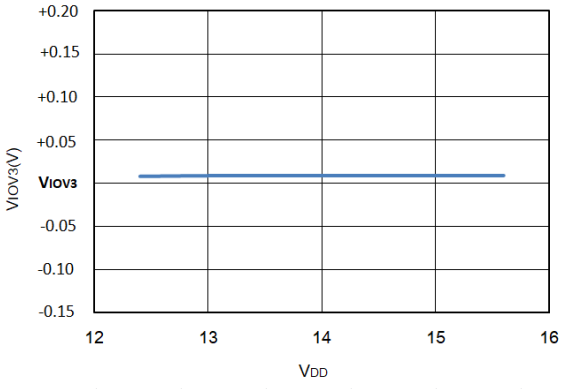
(10) V_{iov2} vs. VDD



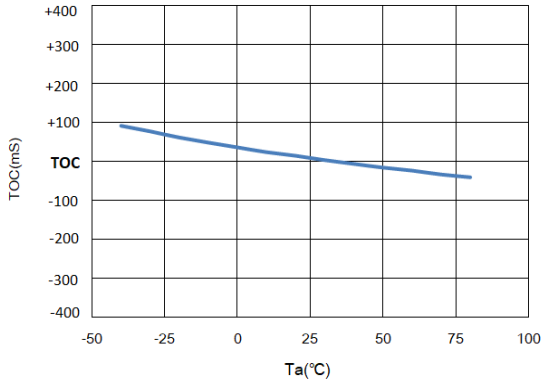
(11) V_{iov3} vs. Ta



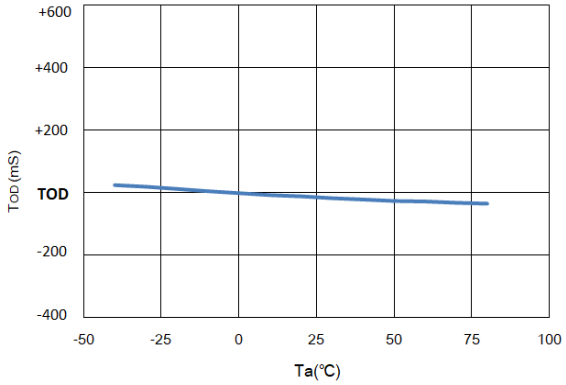
(12) V_{iov3} vs. VDD



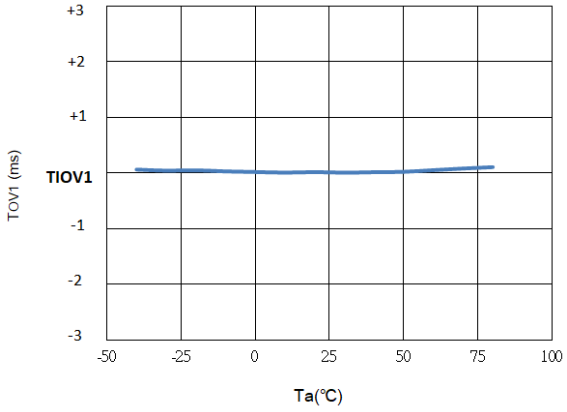
(13) TOC vs. Ta



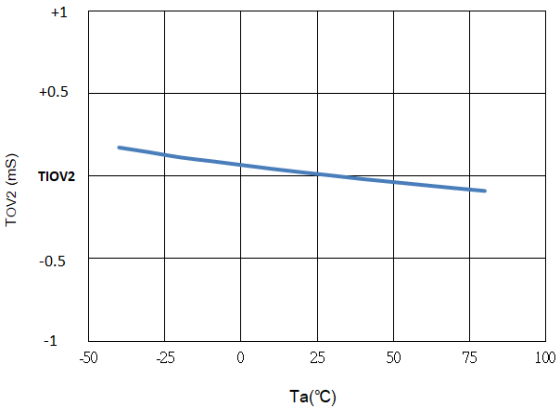
(14) TOD vs.Ta



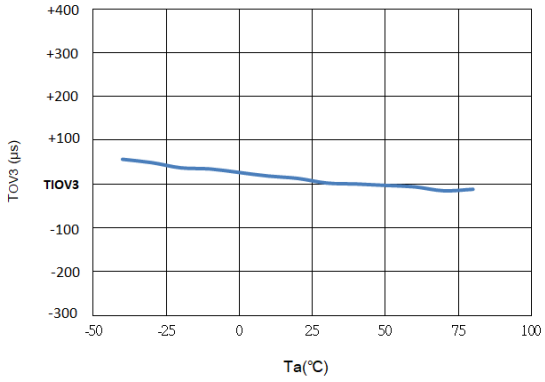
(15) TIOV1 vs. Ta



(16)TIOV2 vs.Ta

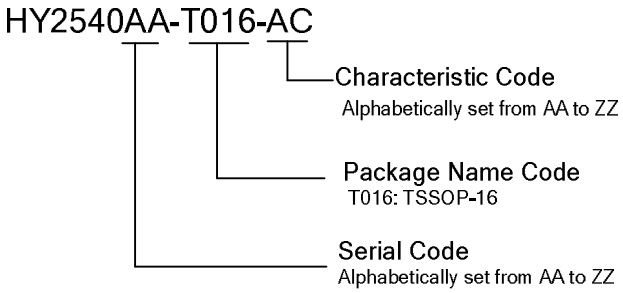


(17) TIOV3 vs.Ta



12. Ordering Information

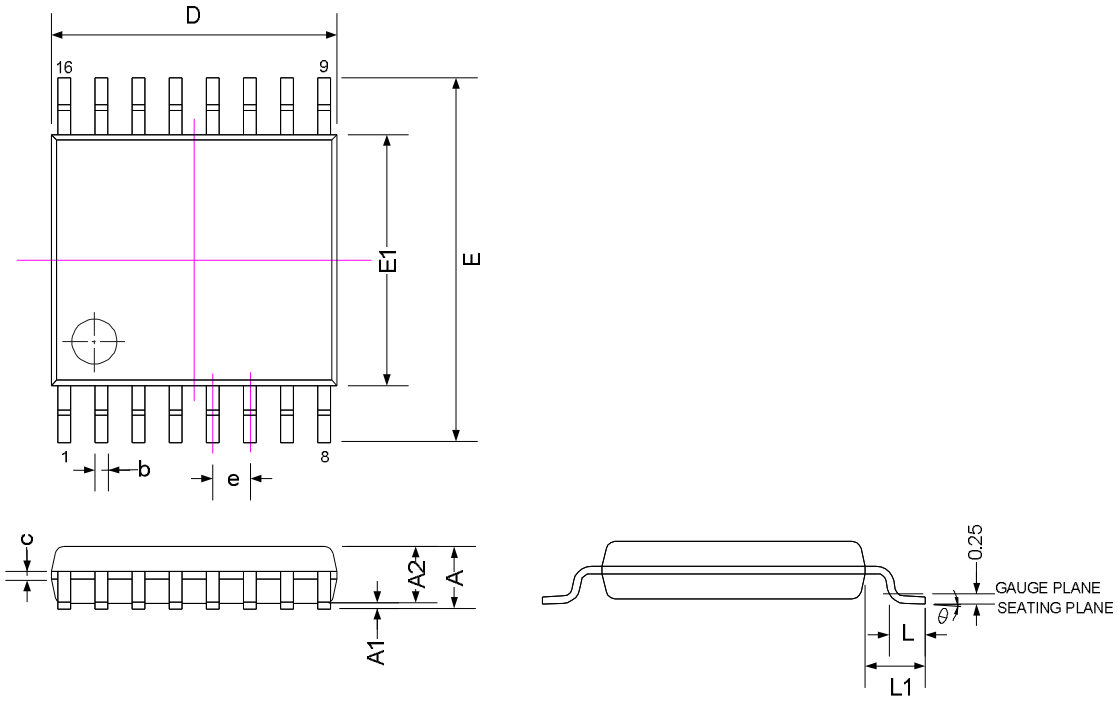
- Product name definition



13. Package Information

13.1. TSSOP-16 Outline

Unit: mm.



SYMBOLS	MIN	NOM	MAX
A	-	-	1.20
A1	0.00	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.40 BSC.		
L	0.45	0.60	0.75
L1	1.0 REF.		
e	0.65 BSC.		
θ°	0	-	8

Note:

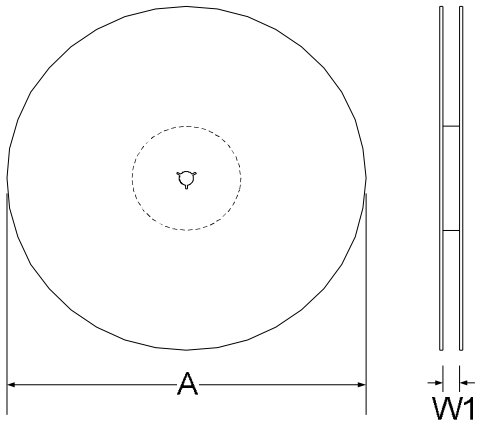
1. All dimensions refer to JEDEC OUTLINE MO -153.
2. Do not include Mold Flash or Protrusions.

14. Tape & Reel Information

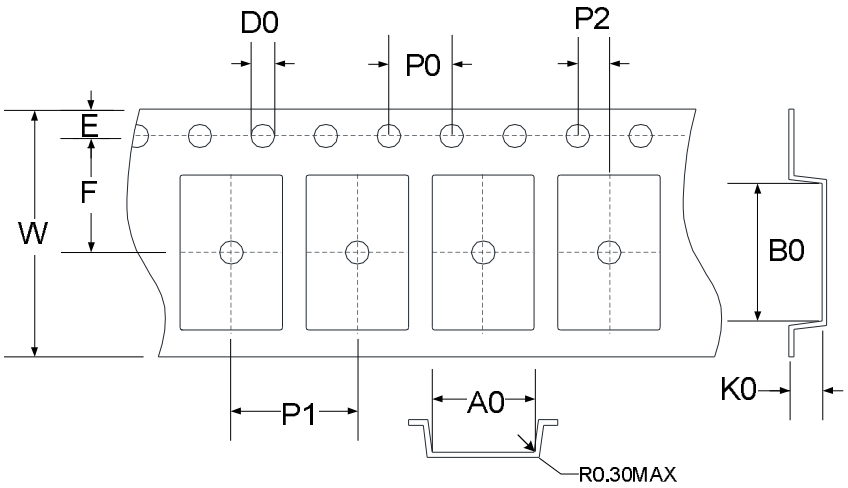
14.1. Tape & Reel Information---TSSOP-16

Unit: mm

14.1.1. Reel Dimensions



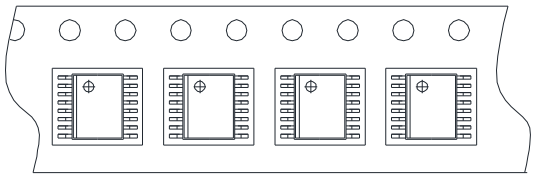
14.1.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	6.80	5.40	1.50	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

14.1.3. PIN1 direction



15. Revision Record

Major differences are stated thereinafter:

Version	Page	Revision Summary
V01	-	First Edition.