



- ★ Low drain-source ON resistance
- ★ Green Device Available
- ★ ESD Protected Embedded

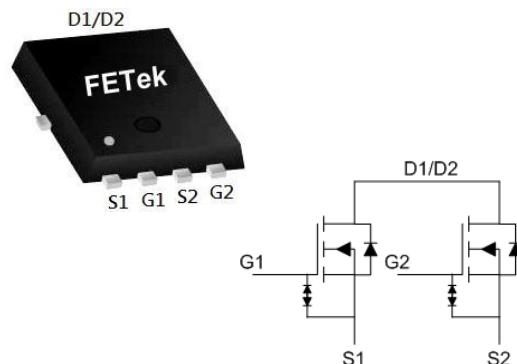
### Product Summary

BVDSS	RDS(ON)	ID
20V	17mΩ	7

### Description

The FKBE2730 is the low RDS(ON) trench N-CH MOSFETs with robust ESD protection. This product is suitable for Lithium-ion battery pack applications. The FKBE2730 meet the RoHS and Green Product requirement with full function reliability approved.

### PRPAK3X3 NEP Pin Configuration



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	20	V
$V_{GS}$	Gate-Source Voltage	$\pm 12$	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current <sup>1</sup>	7	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current <sup>1</sup>	5.8	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	43	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation <sup>3</sup>	1.47	W
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$T_J$	Operating Junction Temperature Range	-55 to 150	°C

### Thermal Data

Symbol	Parameter	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	85	°C/W



FETek Technology Corp.

FKBE2730

N-Ch 20V Fast Switching MOSFETs

Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)

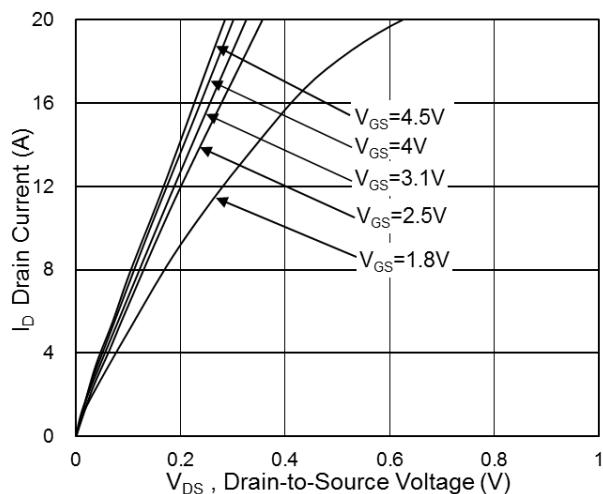
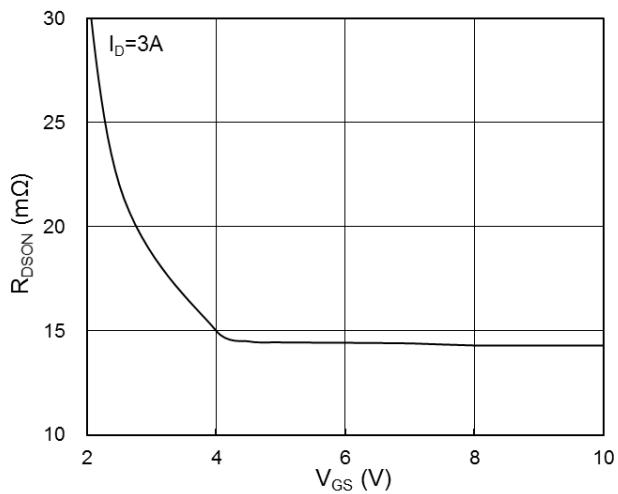
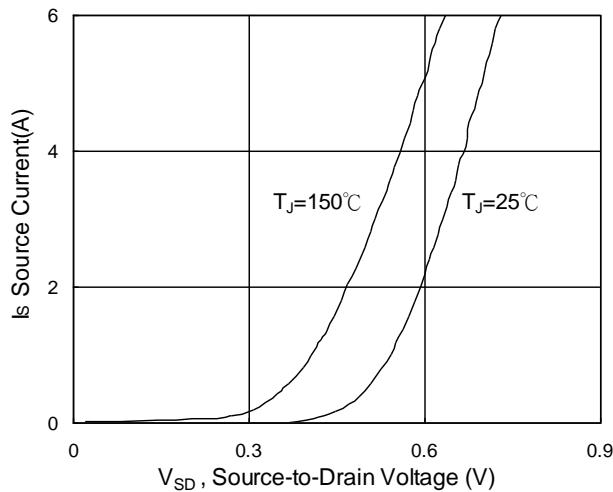
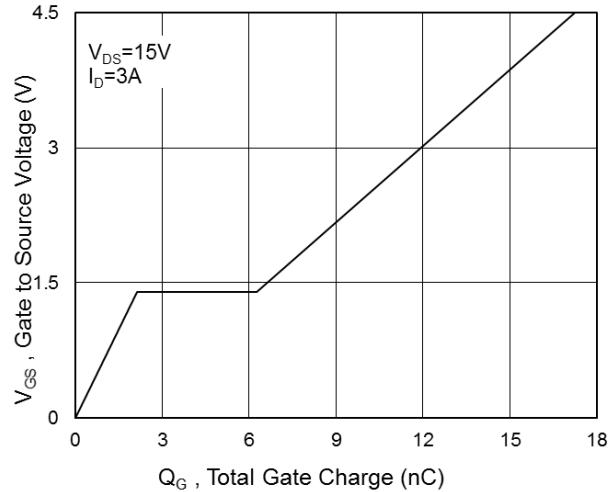
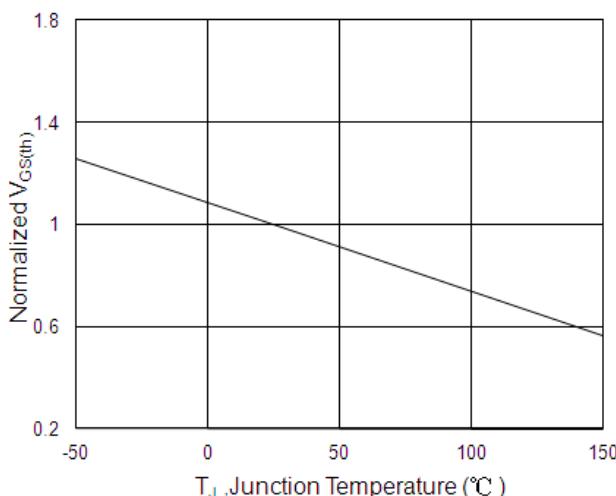
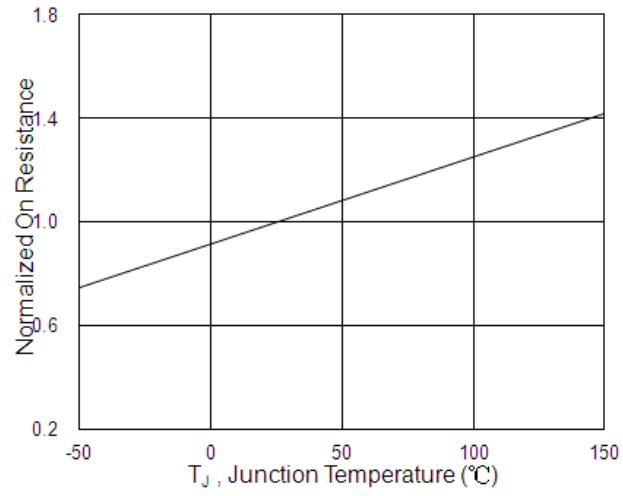
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$ , $I_D=250\mu\text{A}$	20	---	---	V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	BV <sub>DSS</sub> Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$	---	0.014	---	$\text{V}/^\circ\text{C}$
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{\text{GS}}=4.5\text{V}$ , $I_D=3\text{A}$	---	14.5	17	$\text{m}\Omega$
		$V_{\text{GS}}=4.0\text{V}$ , $I_D=3\text{A}$	---	15	18.5	$\text{m}\Omega$
		$V_{\text{GS}}=3.1\text{V}$ , $I_D=3\text{A}$	---	18.5	24.5	$\text{m}\Omega$
		$V_{\text{GS}}=2.5\text{V}$ , $I_D=3\text{A}$	---	22	27	$\text{m}\Omega$
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$ , $I_D=250\mu\text{A}$	0.5	---	1.2	V
$\Delta V_{\text{GS(th)}}$	V <sub>GS(th)</sub> Temperature Coefficient		---	-2.09	---	$\text{mV}/^\circ\text{C}$
$I_{\text{DSS}}$	Drain-Source Leakage Current	$V_{\text{DS}}=16\text{V}$ , $V_{\text{GS}}=0\text{V}$ , $T_J=25^\circ\text{C}$	---	---	25	$\mu\text{A}$
$I_{\text{GSS}}$	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 12\text{V}$ , $V_{\text{DS}}=0\text{V}$	---	---	$\pm 10$	$\mu\text{A}$
$R_g$	Gate Resistance	$V_{\text{DS}}=0\text{V}$ , $V_{\text{GS}}=0\text{V}$ , $f=1\text{MHz}$	---	1.83	---	$\Omega$
$Q_g$	Total Gate Charge (4.5V)	$V_{\text{DS}}=16\text{V}$ , $V_{\text{GS}}=4.5\text{V}$ , $I_D=3\text{A}$	---	9.86	---	nC
$Q_{\text{gs}}$	Gate-Source Charge		---	1.41	---	
$Q_{\text{gd}}$	Gate-Drain Charge		---	2.48	---	
$T_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}}=10\text{V}$ , $V_{\text{GS}}=4.5\text{V}$ , $R_G=3.3\Omega$ , $I_D=3\text{A}$	---	7	---	ns
$T_r$	Rise Time		---	36	---	
$T_{\text{d(off)}}$	Turn-Off Delay Time		---	46.5	---	
$T_f$	Fall Time		---	15	---	
$C_{\text{iss}}$	Input Capacitance	$V_{\text{DS}}=15\text{V}$ , $V_{\text{GS}}=0\text{V}$ , $F=1\text{MHz}$	---	735	---	pF
$C_{\text{oss}}$	Output Capacitance		---	83	---	
$C_{\text{rss}}$	Reverse Transfer Capacitance		---	81	---	

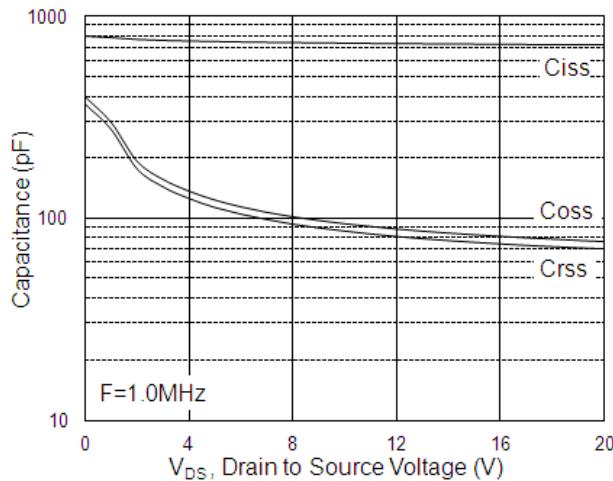
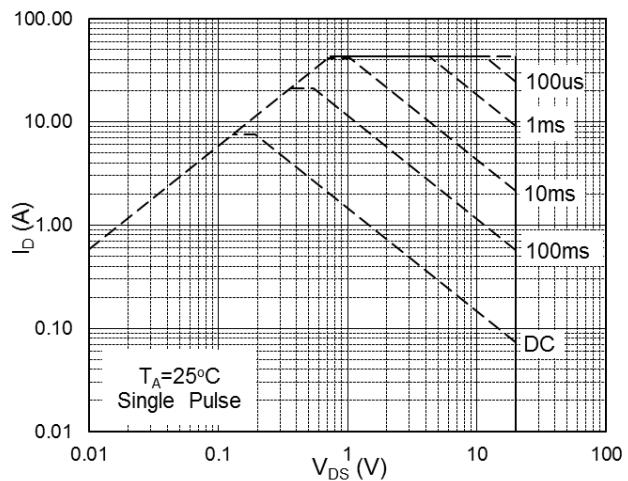
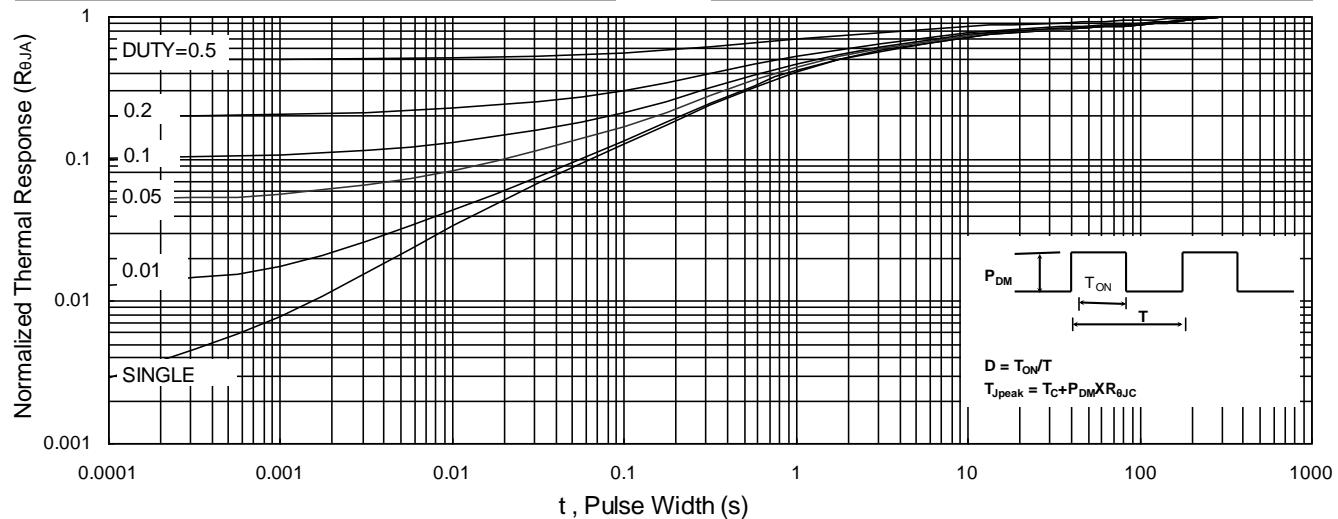
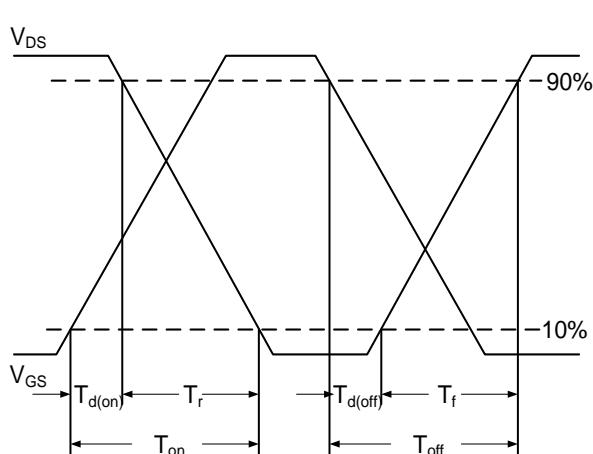
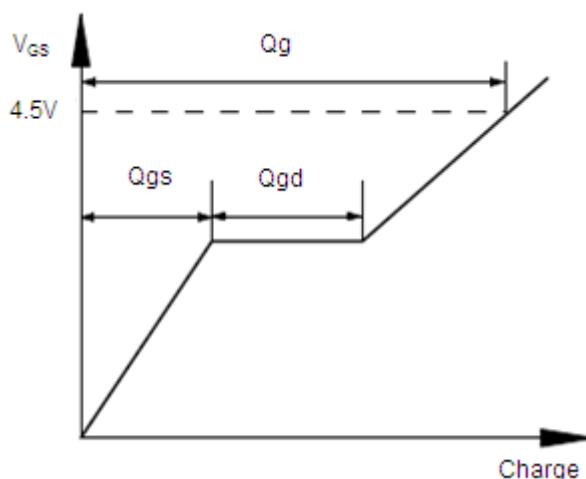
## Diode Characteristics

Symbol	Parameter	Conditions	Max.	Unit
$I_s$	Continuous Source Current <sup>1,6</sup>	$V_G=V_D=0\text{V}$ , Force Current	7	A
$V_{\text{SD}}$	Diode Forward Voltage <sup>2</sup>	$V_{\text{GS}}=0\text{V}$ , $I_s=7\text{A}$ , $T_J=25^\circ\text{C}$	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu\text{s}$  , duty cycle  $\leq 2\%$
- 3.The power dissipation is limited by  $150^\circ\text{C}$  junction temperature.
- 4.The data is theoretically the same as  $I_D$  and  $I_{\text{DM}}$  , in real applications , should be limited by total power dissipation.

**Typical Characteristics**

**Fig.1 Typical Output Characteristics**

**Fig.2 On-Resistance vs. Gate-Source Voltage**

**Fig.3 Forward Characteristics of Reverse**

**Fig.4 Gate-Charge Characteristics**

**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$** 

**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**


**Fig.7 Capacitance**

**Fig.8 Safe Operating Area**

**Fig.9 Normalized Maximum Transient Thermal Impedance**

**Fig.10 Switching Time Waveform**

**Fig.11 Gate Charge Waveform**